This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a first conductivity type layer at a principal surface and a second conductivity type layer at a rear surface[principal surface of a first conductivity type];

a second conductivity type diffusion region, having an island shape, formed at [on] the principal surface of said semiconductor substrate, wherein the second conductivity type diffusion region has an impurity concentration profile resulting from impurities of a second conductive type in a depth direction of the semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type diffusion region wherein said impurity concentration profile of said second conductive type impurity has a plurality of peaks at different depths [conductivity type region changes gently] in the depth direction of the semiconductor substrate such that [and wherein said impurity concentration profile of said second conductivity type region, resulting from impurities of a second conductivity type has] a gentle peak is formed at a depth that is greater than a junction depth of said first conductivity type diffusion region;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type diffusion region through[to at least] said second conductivity type diffusion region to said first conductivity type layer of [on] said semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon filling said trench, such that said insulation film is located between said electrode portion and said inner wall surface.

2. (Original) The semiconductor device according to claim 1, wherein said electrode portion is formed to have a T-shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the semiconductor substrate.

3. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a first conductivity type layer at a principal surface and a second conductivity type layer at a rear surface [principal surface of a first conductivity type];

a second conductivity type diffusion region formed at[on] the principal surface of said semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type diffusion region;

a plurality of first trenches, each extending from a surface of said highly doped first conductivity type region through [to reach at least]said second conductivity type diffusion region to[on] said first conductivity type layer of said semiconductor substrate, thereby defining a channel portion on an inner wall surface of each of the first trenches;

an insulation film formed on the inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon filling each of the first trenches such that said insulation film is located between said electrode portion and said inner wall surface;

a plurality of second trenches formed to extend into but not through said second conductivity type diffusion region so that each of the second trenches is positioned between an adjacent pair of said first trenches;

a second conductivity type protrusion region, which protrudes downwardly, wherein the second conductivity type protrusion region forms a junction that is deeper than a junction of said second conductivity type diffusion region, the protrusion region being positioned beneath the second trench; and

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

4. (Original) The semiconductor device according to claim 3, wherein said electrode portion is formed to have a T-shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the semiconductor substrate.

5. (Original) The semiconductor device according to claim 3, further comprising:

an electrode electrically connecting said highly doped first conductivity type region to said second conductivity type protrusion region through said second trench.

6. (Currently Amended) The semiconductor device according to claim 3, further comprising a portion of the second conductivity type diffusion region disposed between an adjacent pair of the first trenches, where the second trenches are not formed, wherein the portion is in an electrically floating state.

7. (Previously Amended) The semiconductor device according to claim 3, further comprising:

a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the one of the second trenches;

a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the another one of the second trenches, the second electrode being disposed adjacent to the first electrode;

wherein one of adjacent pair of the first and second electrodes is in an electrically floating state.

8. (Previously Amended) The semiconductor device according to claim 5, wherein said second conductivity type highly doped region contacts said electrode, and is disposed between the electrode and the second conductivity type protrusion region.

9. (Currently Amended) The semiconductor device according to claim 5, wherein one of said plurality of first trenches encloses the portion of the second conductivity type diffusion region entirely.

10. (Original) The semiconductor device according to claim 3, wherein each of the first trenches is made shallower than each of the second conductivity type protrusion regions.

11. (Currently Amended) The semiconductor device according to claim 3[1], further comprising:

a plurality of electric field alleviating regions of the second conductivity type formed in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type diffusion region.

12. (Previously Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions is composed of:

a strip-wise third trench; and

a second conductivity type deep region encompassing the strip-wise third trench.

13. (Currently Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions has a pn junction that is deeper than a pn junction of said second conductivity type diffusion region.

14. (Currently Amended) The semiconductor device according to claim 11, wherein said semiconductor device is constituted as a gate driving type power element for controlling a conduction state between the rear [a back]surface of said semiconductor substrate and said highly doped first conductivity type region by using said electrode portion as a control electrode.

15 - 28 were previously canceled without prejudice.

29 - 33 (Cancelled)

34. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, wherein the trench MOS structure includes:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench;

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second trench extending into but not through the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and the protrusion region encompasses the second conductivity type doped region; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench.

35. (Previously Added) The semiconductor device according to claim 34, further comprising a third semiconductor layer of a second conductivity type, the third semiconductor layer being located on a rear surface of the first semiconductor layer, opposite to the second semiconductor layer.

36. (Previously Added) The semiconductor device according to claim 35, further comprising a lower electrode contacting the third semiconductor layer.

37. (Previously Added) The semiconductor device according to claim 34, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

38. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, comprising:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench; and

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer by said first trench and being in an electrically floating state; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through a second trench, wherein the upper electrode is isolated from the second conductivity type island.

39. (Previously Added) The semiconductor device according to claim 38, wherein the trench MOS structure further comprises a second conductivity type protrusion region, the junction depth of which is greater than the junction depth of the second semiconductor layer, and wherein the protrusion region is positioned away from the first trench.

40. (Previously Amended) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises the second trench located in the second conductivity type region and positioned away from the first trench, the protrusion region being positioned beneath the second trench.

41. (Previously Added) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

42. (Previously Added) The semiconductor device according to claim 39, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

43. (Previously Added) The semiconductor device according to claim 38, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

44. (Previously Added) The semiconductor device according to claim 43, further comprising a lower electrode contacting the third semiconductor layer.

45. (Previously Added) The semiconductor device according to claim 39, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

46. (Previously Added) The semiconductor device according to claim 45, further comprising a lower electrode contacting the third semiconductor layer.

47. (Previously Added) The semiconductor device according to claim 41, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

48. (Previously Added) The semiconductor device according to claim 47, further comprising a lower electrode contacting the third semiconductor layer.

49. (Previously Added) The semiconductor device according to claim 42, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

50. (Previously Added) The semiconductor device according to claim 49, further comprising a lower electrode contacting the third semiconductor layer.

51. (Previously Added) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer, wherein the second semiconductor layer is divided into a first portion and a second portion, the second portion being isolated from the first portion;

a first doped region of a first conductivity type located inside the first portion and proximate to an opening of the first trench;

a second doped region of a first conductivity type located inside the second portion and proximate to the opening of the first trench;

an insulation film located on an inner wall of the first trench;

a gate electrode located in the first trench, wherein a first trench MOS structure is collectively formed with the first semiconductor layer, the first portion and the first doped region, and a second trench MOS structure is collectively formed with the first semiconductor layer, the second portion and the second doped region; and

an upper electrode contacting the first doped region and the first portion of the first trench MOS structure, wherein the second doped region and the second portion of the second trench MOS structure are in an electrically floating state.

52. (Previously Added) The semiconductor device according to claim 51, wherein the first trench MOS structure further comprises a second conductivity type protrusion region having a junction depth that is greater than a junction depth of the first portion of the second semiconductor layer, the protrusion region being positioned away from the first trench.

53. (Previously Added) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second trench located away from the first trench, the protrusion region being positioned beneath the second trench.

54. (Previously Added) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region and having a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

55. (Previously Added) The semiconductor device according to claim 52, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

56. (Previously Added) The semiconductor device according to claim 51, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

57. (Previously Added) The semiconductor device according to claim 56, further comprising a lower electrode contacting the third semiconductor layer.

58. (Previously Added) The semiconductor device according to claim 52, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

59. (Previously Added) The semiconductor device according to claim 58, further comprising a lower electrode contacting the third semiconductor layer.

60. (Previously Added) The semiconductor device according to claim 54, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

61. (Previously Added) The semiconductor device according to claim 60, further comprising a lower electrode contacting the third semiconductor layer.

62. (Previously Added) The semiconductor device according to claim 55, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

63. (Previously Added) The semiconductor device according to claim 62, further comprising a lower electrode contacting the third semiconductor layer.